ACADEMIC REGULATIONS

AND

COURSE STRUCTURE

CHOICE BASED CREDIT SYSTEM

MLR17

EMBEDDED SYSTEMS

for

Master of Technology (M.Tech)

M. Tech. - Regular Two Year Degree Program
(For batches admitted from the academic year 2017 - 2018)

MARRI LAXMAN REDDY
GROUP OF INSTITUTIONS

MLR Institute of Technology

(Autonomous)
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FOREWORD

The autonomy is conferred on MLR Institute of Technology by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

MLR Institute of Technology is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college to order to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought, at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

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M. Tech. - Regular Two Year Degree Program
(For batches admitted from the academic year 2017 - 18)

For pursuing two year post graduate Masters Degree Programme of study in Engineering (M.Tech) offered by MLR Institute of Technology under Autonomous status and herein referred to as MLRIT (Autonomous):

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2017-18 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for MLR Institute of Technology (Autonomous).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, MLR Institute of Technology shall be the Chairman, Academic Council.

1. ADMISSION

Admission into first year of two year M. Tech. degree Program of study in Engineering:
Eligibility:

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. From time to time

2. AWARD OF M. Tech. DEGREE

A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after two academic years of course work, failing which he shall forfeit his seat in M. Tech. programme.

The student shall register for all 90 credits and secure all the 90 credits.
The minimum instruction days in each semester are 90.

3. COURSESOFSTUDY

The following specializations are offered at present for the M. Tech. programme of study.

1. Aerospace Engineering
2. CAD/CAM
3. Computer Science and Engineering
4. Digital Systems & Computer Electronics
5. Embedded Systems
6. Thermal Engineering

4. Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice / Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME

Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Subject/ Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Subject (subject to offering of such a Subject), or for another existing Subject (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5. ATTENDANCE

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below75%) in each semester shall be granted by the College Academic Committee.

5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

5.6 A Candidate shall put in a minimum required attendance at least three (3) theory subjects in I Year I semester for promoting to I Year II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission in to the same class.

6. EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

- For the theory subjects 70 marks shall be awarded for the performance in the Semester End Examination and 30 marks shall be awarded for Continuous Internal Evaluation (CIE).

The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other, immediately after the completion of Semester instructions. Each mid-term examination shall be conducted for a total duration of 120 minutes.

Sessional Examinations

- Subjective Paper shall contain three questions. Question 1 & 2 with internal choice from unit-I, question 3 & 4 with internal choice from unit-II and question 5 having a, b questions with internal choice from first half part of unit-III for I-MID examinations. For II-MID 1 & 2 questions from unit-4, questions 3 & 4 from unit-5 and question no 5 from remaining half part of unit-3. The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus.
- The Semester End Examination will be conducted for 70 marks examination shall be conducted for a total duration of 180 minutes. Question paper consists of Part –A and Part-B with the following.
- Part-A is a compulsory question consisting of 5 questions, one from each unit and carries 4 marks each.
- Part-B to be answered 5 questions carrying 10 marks each. There will be two questions from each unit and only one should be answered.

6.1 For practical subjects, 70 marks shall be awarded for performance in the Semester End Examinations and 30 marks shall be awarded for day-to-day performance as Internal Marks.

6.2 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and the same to be informed to the Chief Controller of Examination in two weeks before for commencement of the lab end examinations.

6.3 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50%ofmarks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Head of the Department shall be associated with the conduct of the Comprehensive Viva-Voce through a Committee. The Committee consisting of Head of the Department, one senior faculty member and an external examiner. The external examiner shall be appointed by the Chief Controller of Examinations. For this, the HOD of the department shall submit a panel of 3 examiners. There are no internal marks for the Comprehensive Viva-Voce and evaluates for maximum of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6.6) he has to re appear for the Semester End Examination in that subject.

6.7 A candidate shall be given one chance to re-register for the subjects if the internal marks secured by a candidate is less than 50% and failed in that subject for maximum of two subjects and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the subjects and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those subjects. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stands cancelled.

6.8 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the Semester End Examination in that subject. He shall re-register for the subject when next offered.

7. Examinations and Assessment - The Grading System

7.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item6above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	***Letter Grade (UGC Guidelines)***	***Grade Points***
90% and above (≥ 90% , ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥ 80% , < 90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥ 70% , < 80%)	A (Very Good)	8
Below 70% but not less than 60% (≥ 60% , < 70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50% , < 60%)	B (above Average)	6
Below 50% but not less than 40% (≥ 40% , < 50%)	C (Average)	5
Below 40% (< 40%)	F (FAIL)	0
Absent	AB	0

7.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then 'AB' Grade will be allocated in any Subject shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA / CGPA Improvement'.

7.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject / Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.8 The Student passes the Subject/ Course only when he **gets GP □□6 (B Grade or above).**

7.9 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/Course (excluding Mandatory non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.10 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP)secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

SGPA = $\{\sum_{i=1}^{N} C_i G_i\} / \{\sum_{i=1}^{N} C_i\}$ …. For each Semester,

where 'i' is the Subject indicator index (takes into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to that ix Subject, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that ith Subject.

Illustration of Computation of SGPA

Course	Credit	Grade Letter	Grade Point	Credit Point (Credit x Grade)
Course1	3	A	8	3 x 8 = 24
Course2	4	B+	7	4 x 7 = 28
Course3	3	B	6	3 x 6 = 18
Course4	3	O	10	3 x10= 30
Course5	3	C	5	3 x 5 = 15
Course6	4	B	6	4 x 6 = 24

Thus, **SGPA =139/20 =6.95**

7.11 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

CGPA = $\{\sum_{j=1}^{M} C_j G_j\} / \{\sum_{j=1}^{M} C_j\}$ … for all S Semesters registered

(i.e., up to and inclusive of S Semesters, S ≥ 2)

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the jth Subject, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for

that jth Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

For CGPA Computation

Semester 1	Semester 2	Semester 3	Semester 4	Semester 5	Semester 6
Credits : 20 SGPA : 6.9	Credits : 22 SGPA : 7.8	Credits : 25 SGPA : 5.6	Credits : 26 SGPA : 6.0	Credits : 26 SGPA : 6.3	Credits : 25 SGPA : 8.0

Thus, **CGPA =** $\frac{20 \times 6.9 + 22 \times 7.8 + 25 \times 5.6 + 26 \times 6.0 + 26 \times 6.3 + 25 \times 8.0}{144} = 6.73$

7.12 For Calculations listed in Item 7.6 – 7.10, performance in failed Subjects/ Courses (securing F Grade) will also be taken into account, and the Credits of such Subjects/ Courses will also be included in the multiplications and summations.

8. EVALUATIONOFPROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the Examination Branch for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 30%, then only thesis will be accepted for submission.

8.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

8.9 For Project work Review I in II Year I Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work and Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Phase-I. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

8.10 For Project Phase-II in II Year II Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The PRC will examine the overall progress of the Project Work and decide the Project is eligible for final submission or not. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review II. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

8.11 For Project Evaluation (Viva Voce) in II Year II Sem. there is an external marks of 150 and the same evaluated by the External examiner appointed by the Chief Controller of Examinations. The candidate has to secure minimum of 50% marks in Project Dissertation.

8.12 If he fails to fulfill as specified in 8.11, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

8.13 The thesis shall be adjudicated by one examiner selected by the Chief Controller of Examinations. For this, the HOD of the Department shall submit a panel of 3 examiners, eminent in that field, with the help of the guide concerned and Head of the Department.

8.14 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

8.15 If the report of the examiner is favorable, Project dissertation shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.16 The Head of the Department shall coordinate and make arrangements for the conduct of Project dissertation.

9. AWARD OFDEGREEAND CLASS

9.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 90 Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	Grade to be Secured
First Class with Distinction	CGPA ≥ 8.00
First Class	≥ 7.00 to < 8.00 CGPA
Second Class	≥ 6.00 to < 7.00 CGPA

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. WITHOLDING OF RESULTS

If the student has not paid the dues, if any, to the college or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be with held in such cases.

11. TRANSITORY REGULATIONS

11.1 If any candidate is detained due to shortage of attendance in one or more subjects, they are eligible for re-registration to maximum of two earlier or equivalent subjects at a time as and when offered.

11.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per MLR17 Academic Regulations.

12. GENERAL

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

12.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

MALPRACTICES RULES
DISCIPLINARY ACTIONFOR / IMPROPER CONDUCT IN EXAMINATIONS

S. No	Nature of Malpractices/Improper conduct	Punishment
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s)who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

COURSE STRUCTURE

EMBEDDED SYSTEMS
M.Tech.-COURSE STRUCTURE - MLR-17

I semester								
Code	**Course Title**	**Periods per week**			**Credits**	**Scheme of Examination Maximum marks**		
		L	**T**	**P**		**Int. Marks**	**Ext. Marks**	**Total**
B25501	Embedded System Design	4	--		4	**30**	**70**	**100**
B25502	VLSI Technology and Design	4	--		4	**30**	**70**	**100**
B25503	Embedded Real time operating systems	4	--		4	**30**	**70**	**100**
	Core Elective I	4	--		4	**30**	**70**	**100**
	Core Elective II	4	--		4	**30**	**70**	**100**
	Open Elective I	4	--		4	**30**	**70**	**100**
B25513	Embedded C laboratory	--	--	4	2	**30**	**70**	**100**
B25514	**Seminar**	--	--	4	2	**50**	--	**50**
Total		**24**		**8**	**28**	**260**	**490**	**750**

II semester								
Code	**Course Title**	**Periods per week**			**Credits**	**Scheme of Examination Maximum marks**		
		L	**T**	**P**		**Int. Marks**	**Ext. Marks**	**Total**
B25515	Digital Signal Processors and Architectures	4	--		4	**30**	**70**	**100**
B25516	Embedded Networking	4	--		4	**30**	**70**	**100**
B25517	Low power VLSI design	4	--		4	**30**	**70**	**100**
	Core Elective III	4	--		4	**30**	**70**	**100**
	Core Elective IV	4	--		4	**30**	**70**	**100**
	Open Elective II	4	--		4	**30**	**70**	**100**
B25527	Advanced Embedded Systems Lab	--	--	**4**	**2**	**30**	**70**	**100**
B25528	**Seminar**	--	--	**4**	**2**	**50**	--	**50**
Total		**24**		**8**	**28**	**260**	**490**	**750**

III semester								
Code	**Course Title**	**Periods per week**			**Credits**	**Scheme of Examination Maximum marks**		
		L	**T**	**P**		**Int. Marks**	**Ext. Marks**	**Total**
B25529	Comprehensive Viva -Voce	-	--		4	-	100	100
B25530	Project Phase –I	-	--		12	50	-	50
TOTAL					**16**	**50**	**100**	**150**

IV semester								
Code	**Course Title**	**Periods per week**			**Credits**	**Scheme of Examination Maximum marks**		
		L	**T**	**P**		**Int. Marks**	**Ext. Marks**	**Total**
B25531	Project Phase –II & Dissertation	-	--		18	50	150	200
TOTAL					**18**	**50**	**150**	**200**

OPEN ELECTIVES			
OE1		**OE2**	
B25510	Embedded C	B25524	Design for testability
B25511	Advanced Data Communication	B25525	Advanced Computer Architecture
B25512	Microcontrollers for Embedded System Design	B25526	Wireless LANs and PANs

CORE ELECTIVES			
CE1		**CE2**	
B25504	Digital System Design	B25507	Hardware Software Codesign
B25505	Sensors and Actuators	B25508	Embedded Computing
B25506	Soft Computing Techniques	B25509	Image and Video Processing
CE3		**CE4**	
B25518	Network Security and cryptography	B25521	CPLD and FPGA Architectures and applications
B25519	Internetworking	B25522	System on chip architecture
B25520	Wireless Communication and networks	B25523	Advanced Operating systems

I M.TECH I SEMESTER

SYLLABUS

EMBEDDED SYSTEMS DESIGN

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25501 **4 - - 4**

UNIT -I

Introduction to Embedded Systems : Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System : Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs,Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to thetype of Interface, Memory hadowing, Memory selection for Embedded Systems, Sensors andActuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real T ime Clock, Watchdog Timer,Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets,Task Synchronization: Task Communication/Synchronization Issues, Task SynchronizationTechniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS :

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

VLSI TECHNOLOGY AND DESIGN

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25502- **4 - - 4**

UNIT –I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology,Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts : Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

EMBEDDED REAL TIME OPERATING SYSTEMS

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25503- **4 - - 4**

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read,write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization,Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real TimeClocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS:RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, Tiny OS and Basic Concepts of Android OS.

TEXT BOOKS:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

DIGITAL SYSTEM DESIGN
(Core Elective -I)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25504 **4 - - 4**

UNIT -I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machineminimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cyclesand Hazards.

UNIT -II

Digital Design: Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner,Binary divider.

UNIT -III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of BinaryMultiplier, dice game controller.

UNIT -IV

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Faultdominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Randomtesting, Transition count testing, Signature analysis and test bridging faults
.

UNIT -V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

IMAGE AND VIDEO PROCESSING
(Core Elective-II)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25509 **4 - - 4**

UNIT –I

Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT –III

Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, , Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV

Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang.1st Ed., PH Int.

REFRENCE BOOKS:

1. Digital Image Processing and Analysis-Human and Computer Vision Application with CVIPTools – Scotte mbaugh, 2nd Ed, CRC Press, 2011.
2. Digital Video Processing – M. Tekalp, Prentice Hall International.
3. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009.
4. Multidimentional Signal, Image and Video Processing and Coding – John Woods, 2nd Ed,Elsevier.
5. Digital Image Processing with MATLAB and Labview – Vipula Singh, Elsevier.
6. Video Demystified – A Hand Book for the Digital Engineer – Keith Jack, 5th Ed., Elsevier.

SOFT COMPUTING TECHNIQUES
(Core Elective -I)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25506 **4 - - 4**

UNIT –I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuronmodel, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning andTraining the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzyknowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Selforganizingfuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters,Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT –V

Applications: GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House,1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt.Ltd., 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan,Sanjay Ranka, Penram International.
6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.
7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

HARDWARE - SOFTWARE CO-DESIGN
(Core Elective II)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25507 **4 - - 4**

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, KluwerAcademic Publishers

REFERENCE BOOKS:

A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

EMBEDDED COMPUTING
(Core Elective – II)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25508 **4 - - 4**

UNIT –I

Programming on Linux Platform: System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box.

Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore,Message Queue.

UNIT –II

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimizationswitches, lint, code profiling tools,.

UNIT –III

Interfacing Modules: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT –IV

Networking Basics: Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee,SSH, firewalls, network security.

UNIT –V

IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens.

SENSORS AND ACTUATORS
(Core Elective –II)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25509 **4 - - 4**

UNIT -I

Sensors / Transducers: Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization.

Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors.

UNIT –II

Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors.

UNIT -III

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors

UNIT -IV

Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart SensorInterface – The Automation.

UNIT -V

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains.

TEXT BOOKS:

1. D. Patranabis – “Sensors and Transducers” –PHI Learning Private Limited.
2. W. Bolton – “Mechatronics” –Pearson Education Limited.

REFERENCE BOOKS

1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

EMBEDDED C
(Open Elective-I)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25510 **4 - - 4**

UNIT – I

Programming Embedded Systems in C : Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family : Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT – II

Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III

Adding Structure to the Code : Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV

Meeting Real-Time Constraints : Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V

Case Study: Intruder Alarm System : Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008

REFERENCE BOOKS:

PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C – Nigel Gardner

ADVANCED DATA COMMUNICATIONS
(Open Elective-I)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25511 **4 - - 4**

UNIT -I

Digital Modulation Schemes: BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT -II

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication Networks, Protocols and Standards, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes, Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/IP Protocol suite and Comparison with OSI model.

UNIT -III

Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code

Data Link Control: Line Discipline, Flow Control, Error Control

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols, Bit-Oriented Protocol, Link Access Procedures.

UNIT -IV

Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, DSL.

Local Area Networks: Ethernet, Other Ether Networks, Token Bus, Token Ring, FDDI.

Metropolitan Area Networks: IEEE 802.6, SMDS

Switching: Circuit Switching, Packet Switching, Message Switching.

Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.

UNIT -V

Multiple Access Techniques: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization, Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access(TDMA), Code - Division Multiple Access (CDMA), OFDM and OFDMA.

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 2nd Ed., 2003,TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5th Ed., 2008, PEI.

REFERENCE BOOKS:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th Ed., 2007, PHI.
3. Data Communication and Tele Processing Systems -T. Housely, 2nd Ed, 2008, BSP.
4. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2005, PHI.

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN
(Open Elective-I)

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25512 **4 - - 4**

UNIT –I

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II

ARM Programming Model – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III

ARM Programming Model – II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT –IV

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

EMBEDDED C LABORATORY

M. Tech – I Year – I Sem.(ES) **L T P C**

Sub. Code- B25513 **- - 4 2**

Note:

Minimum of 10 experiments have to be conducted. The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise Directions
11. Program to Sort RTOS on to 89C51 development board.
12. Program to interface Elevator.

I M.TECH II SEMESTER

SYLLABUS

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25515 **4 - - 4**

UNIT –I

Introduction to Digital Signal Processing: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT –II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming.

UNIT –IV

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ,ISBN 0750679123, 2005

EMBEDDED NETWORKING

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25516- **4 - - 4**

UNIT –I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

UNIT –II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables,Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet : Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing a Centric routing.

TEXT BOOKS :

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port -Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.

LOW POWER VLSI DESIGN

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25517 **4 - - 4**

UNIT –I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS :

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.

NETWORK SECURITY AND CRYPTOGRAPHY
(Core Elective – III)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25518 **4 - - 4**

UNIT –I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT –II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT –III

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT –IV

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. **Digital signatures and Authentication Protocols**: Digital signatures, AuthenticationProtocols, Digital signature standards.

Authentication Applications: Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT –V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security: Web Security requirements, Secure sockets layer and Transport layer security,Secure Electronic Transaction.

Intruders, Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

REFERENCE BOOKS:

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.
4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

INTERNETWORKING
(Core Elective - III)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25519 **4 - - 4**

UNIT -I

Internetworking Concepts : Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of the Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address:

Classful Addressing : Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting

Classless Addressing: Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.

UNIT -II

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.

Transmission Control Protocol (TCP):TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control. **Mobile IP:** Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP

UNIT -III

Unicast Routing Protocols (RIP, OSPF, and BGP: Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.

Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

UNIT -IV

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet. **Remote Login TELNET:** Concept, Network Virtual Terminal (NVT). **File Transfer FTP and TFTP:** File Transfer Protocol (FTP). **Electronic Mail:** SMTP and POP. **Network Management-SNMP:** Concept, Management Components, World Wide Web- HTTP Architecture.

UNIT -V

Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3rd Edition PHI

REFERENCE BOOKS:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.
5. The Internet and Its Protocols – Adrin Farrel, Elsevier, 2005.

WIRELESS COMMUNICATIONS AND NETWORKS
(Core Elective –III)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25520 **4 - - 4**

UNIT -I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT –II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction.

UNIT –III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time,

UNIT -IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm.

UNIT -V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

TEXT BOOKS:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.

REFERENCE BOOKS:

1. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
3. Wireless Communication and Networking – William Stallings, 2003, PHI.
4. Wireless Communication – Upen Dalal, Oxford Univ. Press
5. Wireless Communications and Networking – Vijay K. Gary, Elsevier.

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(Core Elective – IV)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25521 **4 - - 4**

UNIT-I

Introduction to Programmable Logic Devices : Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays : Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs : Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs : Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS :

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad,Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

SYSTEM ON CHIP ARCHITECTURE
(Core Elective -IV)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25522 **4 - - 4**

UNIT –I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II

Processors : Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing PipelineDelays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions,VLIW Processors, Superscalar Processors.

UNIT –III

Memory Design for SOC : Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV

Interconnect Customization and Configuration : Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models,Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: Anoverview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

ADVANCED OPERATING SYSTEMS
(Core Elective -IV)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25523 **4 - - 4**

UNIT –I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II

Introduction to UNIX and LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

UNIT –III

System Calls: System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication : Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

DESIGN FOR TESTABILITY
(Open Elective-II)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25524 **4 - - 4**

UNIT -I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern eneration, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BISTSystems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS :

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L.Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS :

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

ADVANCED COMPUTER ARCHITECTURE
(Open Elective-II)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25525 **4 - - 4**

UNIT -I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT –II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtualmemory.

UNIT -III

Instruction Level Parallelism (ILP) - The Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS :

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS :

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

WIRELESS LANs AND PANs
(Open Elective-II)

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25526 **4 - - 4**

UNIT –I

Wireless System & Random Access Protocols: Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, SlottedALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT –II

Wireless LANs: Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III

The IEEE 802.11 Standard for Wireless LANs: Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT –IV

Wireless PANs: Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks,Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues,Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics SlotAssigment, Scatternet formation.

UNIT –V

The IEEE 802.15 working Group for WPANs: The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and networktopologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS:

1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific, 2011.
2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

REFERENCE BOOKS:

1. Wireless Networks - Kaveh Pahlaram, Prashant Krishnamurthy, PHI, 2002.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, Cengage Learning, 2007.

ADVANCED EMBEDDED SYSTEMS LAB

M. Tech – I Year – II Sem.(ES) **L T P C**

Sub. Code- B25527 **- - 4 2**

Note:

A. The following programs are to be implemented on ARM based Processors/Equivalent.

B. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I:

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   Addition | Subtraction | Multiplication | Division
2. Operating Modes, System Calls and Interrupts Loops, Branches
3. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
4. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
5. Program for reading and writing of a file
6. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
7. Program to demonstrates a simple interrupt handler and setting up a timer
8. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
9. Program to Interface 8 Bit LED and Switch Interface
10. Program to implement Buzzer Interface on IDE environment
11. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
12. Program to demonstrate I2C Interface on IDE environment
13. Program to demonstrate I2C Interface – Serial EEPROM
14. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
15. Generation of PWM Signal
16. Program to demonstrate SD-MMC Card Interface.

PART- II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.